

Product Specification

400G QSFP-DD Active Optical Cable

FCBR850QE2Cyy-1Y FCBN850QE2Cyy-1Y

PRODUCT FEATURES

- Hot-pluggable QSFP-DD Type 2 form factor
- Parallel active optical cable with Eight independent channels
- Multirate capability: 50 Gb/s PAM4 or 25 Gb/s NRZ per channel
- 8x50G PAM4 retimed 400GAUI-8 electrical interface
- Reliable VCSEL array technology using multimode fiber
- Low power dissipation: Typical ~8W
- Single 3.3V power supply
- Commercial operating case temperature range: 0°C to 70°C
- RoHS Compliant



APPLICATIONS

- 400G Ethernet (8x50Gbps)
- 200G Ethernet (8x25Gbps)

PRODUCT SELECTION (Standard Lengths*)

FCBx850QE2Cyy-1Y

x: N for OFNP cable; R for OFNR/LSZH cable

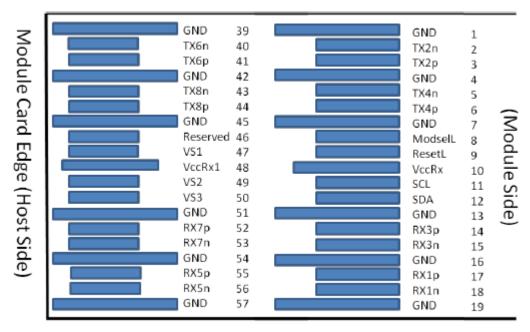
E: Ethernet datarate

C: Commercial temperature range

yy: cable length from 0.5 to 100 meters

^{*}For availability of additional cable lengths or cable types, please contact Coherent.

I. Pin Descriptions



Bottom side viewed from bottom

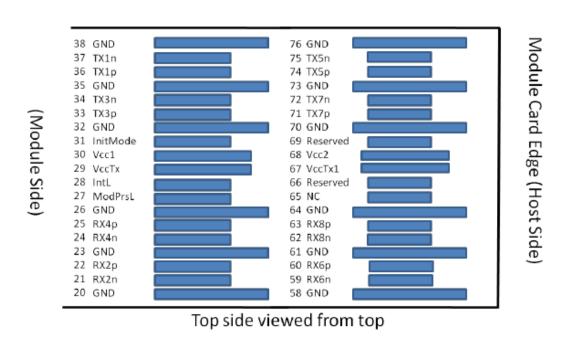


Figure 1 – QSFP-DD -compliant 76-pin connector (per QSFP-DD MSA)

Logic	Symbol	Description	Plug	Notes
	-2		Sequence ⁴	
	GND	Ground	1B	1
CML-T	Tx2n	Transmitter Inverted Data Input	3B	
0.1.2 2	-			1
CMT - T				1
CML-I	-	-		_
				1
LVTTL-I				
	VccRx		2B	2
LVCMOS- I/O	SCL	2-wire serial interface clock	3B	
LVCMOS-	SDA	2-wire serial interface data	3B	
-,-	GND	Ground	1B	1
CMTO				-
	-	-		
CMT-0				
71/T 2				1
	-			
CML-0	Rxln			
	GND	Ground	1B	1
	GND	Ground	1B	1
CML-0	Rx2n	Receiver Inverted Data Output	3B	
CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
	GND	Ground	1B	1
CMTO	Dx4n	Receiver Inverted Data Output	3B	
3.12 0	-			1
TIPET C				1
LVTTL-0		-		_
				2
				2
LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
	GND	Ground	1B	1
CML-I	ТхЗр	Transmitter Non-Inverted Data Input	3B	
CML-I	Tx3n		3B	
				1
CMTT				
	•			
OHL I		•		1
		GIOGHA		_
	GND	Ground	1A	1
CML-I	Tx6n	Transmitter Inverted Data Input	3A	
CML-I	Тибр	Transmitter Non-Inverted Data Input	3A	
	GND	Ground	1A	1
CML-I				_
	•			
J.12 I		•		1
				3
				3
	VccRxl	3.3V Power Supply	2A	2
	VS2 Module Vendor Specific 2		3A	3
	VS3	Module Vendor Specific 3	3A	3
	GND Ground			1
	GND	Ground	1A	1
CML-0	GND Rx7p	Receiver Non-Inverted Data Output	JA JA	1
				1
CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	1
	LVCMOS- I/O LVCMOS- I/O CML-O CML-I CML-I CML-I CML-I CML-I CML-I CML-I	CML-I Tx2n CML-I Tx2p GND CML-I Tx4n CML-I Tx4p GND LVTTL-I ModSelL LVTTL-I ResetL VccRx LVCMOS- SCL I/O LVCMOS- SDA I/O GND CML-O Rx3p CML-O Rx1n GND CML-O Rx1n GND CML-O Rx2n CML-O Rx2n CML-O Rx2n CML-O Rx2n CML-O Intl VccTx VccTx VccI LVTTL-I InitMode GND CML-I Tx3n GND CML-I Tx1n GND CML-I Tx1n GND CML-I Tx6n GND CML-I Tx6n CML-I Tx6n	CML-I Tx2p Transmitter Inverted Data Input CML-I Tx2p Transmitter Non-Inverted Data Input CML-I Tx4p Transmitter Inverted Data Input CML-I Tx4p Transmitter Inverted Data Input CML-I Tx4p Transmitter Non-Inverted Data Input CML-I Tx4p ModSelL Module Select LVTIL-I ModSelL Module Reset VCcRx +3.3V Power Supply Receiver LVCMOS- SCL 2-wire serial interface clock LVCMOS- SCL 2-wire serial interface data LVCMOS- SDA 2-wire serial interface data LVCMOS- SDA 2-wire serial interface data LVCMOS- SDA Ground CML-O Rx3p Receiver Non-Inverted Data Output CML-O Rx3n Receiver Inverted Data Output CML-O Rx1p Receiver Inverted Data Output CML-O Rx1n Receiver Inverted Data Output CML-O Rx2n Receiver Inverted Data Output CML-O Rx2n Receiver Inverted Data Output CML-O Rx2n Receiver Inverted Data Output CML-O Rx4n Receiver Inverted Data Output CML-O Intl Interrupt UCCL-O Intl Interrupt UCCL-O Intl Interrupt UCCL +3.3V Power supply transmitter Vccl +3.3V Power supply LVTIL-I Initmode Initialization mode; In legacy QSFP applications, the Initmode pad is called LPMODE CML-I Tx3p Transmitter Non-Inverted Data Input CML-I Tx3p Transmitter Inverted Data Input CML-I Tx1p Transmitter Inverted Data Input CML-I Tx1p Transmitter Inverted Data Input CML-I Tx6p Transmitter Inverted Data Input CML-I Tx6p Transmitter Inverted Data Input CML-I Tx6p Transmitter Inverted Data Input CML-I Tx8p Transmitter Inverted	CML-I Tx2n Transmitter Inverted Data Input 38 CML-I Tx2p Transmitter Non-Inverted Data Input 38 CMD Ground 18 CML-I Tx4n Transmitter Inverted Data Input 38 CML-I Tx4p Transmitter Non-Inverted Data Input 38 CML-I Tx4p Transmitter Non-Inverted Data Input 38 LVTIL-I Modelle Select 38 18 LVTTL-I Modelle Reset 38 38 LVCMOS-I SCL 2-wire serial interface clock 38 I/O SCL 2-wire serial interface data 38 I/O SDA 2-wire serial interface data 38 I/O SND Ground 18 CML-O Rx3n

56	56 CML-0 Rx5n Receiver Inverted Data Output 3A					
57		GND	Ground	1A	1	
58		GND	Ground	1A	1	
59	CML-O	Rx6n	Receiver Inverted Data Output	3A		
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A		
61		GND	Ground	1A	1	
62	CML-O	Rx8n	Receiver Inverted Data Output	3A		
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A		
64		GND	Ground	1A	1	
65		NC	No Connect	3A	3	
66		Reserved	For future use	3A	3	
67		VccTxl	3.3V Power Supply	2A	2	
68		Vcc2	3.3V Power Supply	2A	2	
69		Reserved	or Future Use 3A 3			
70		GND	round 1A 1			
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A		
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A		
73		GND	round 1A 1			
74	CML-I	Тх5р	ransmitter Non-Inverted Data Input 3A			
75	CML-I	Tx5n	Transmitter Inverted Data Input 3A			
76	76 GND Ground 1A 1					
Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.						
Note 2: VccRx, VccRxl, Vccl, Vcc2, VccTx and VccTxl shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 4. VccRx, VccRxl, Vccl, Vcc2, VccTx and VccTxl may be internally connected within the module in any combination. The connector Vcc pins are each						

rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

II. **Absolute Maximum Ratings**

Module performance is not guaranteed beyond the operating range (see Section V). Exceeding the limits below may damage the transceiver module permanently.

Parameter	Symbol	Min	Тур	Max	Unit	Ref.
Maximum Supply Voltage	Vcc	-0.5		4.0	V	
Storage Temperature	T_{S}	-40		+85	°C	1
Case Operating Temperature	T_{OP}	0		+70	°C	
Relative Humidity	RH	15		85	%	2

- Assumes no mechanical load force on the unit. Ensuring no mechanical load force requires a cable bend radius of >74 mm.
- 2. Non-condensing.

III. Electrical Characteristics (EOL, $T_{OP} = 0$ to +70 °C, $V_{CC} = 3.135$ to 3.465 Volts)

NOTE: The Active Optical Cable requires an electrical connector compliant with the QSFP-DD MSA be used on the host board to guarantee its electrical interface specification. Please check with your connector supplier.

Parameter	Symbol	Min	Тур	Max	Unit	Ref.
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Current	Icc			2.711	A	
Module total power	P			8.5	W	1
Transmitter						
Signaling rate per lane			$625 \pm 100 \text{ p}$	pm.	Gbd	
Differential data input voltage per lane	Vin,pp,diff	900			mV	2
Differential input return loss			quation (83) EEE802.3br		dB	
Differential to common mode input return loss			quation (83 EEE802.3br		dB	
Differential termination mismatch				10	%	
Module stress input test			er 120E.3.4. EEE802.3bs			3
Single-ended voltage tolerance range		-0.4		3.3	V	
DC common mode voltage		-350		2850	mV	4
Receiver						
Signaling rate per lane		26.5	625± 100 p	pm.	Gbd	
AC common-mode output voltage (RMS)				17.5	mV	
Differential output voltage				900	mV	
Near-end ESMW (Eye symmetry mask width)			0.265		UI	
Near-end Eye height, differential (min)		70			mV	
Far-end ESMW (Eye symmetry mask width)			0.2		UI	
Far-end Eye height, differential (min)		30			mV	
Far-end pre-cursor ISI ratio		-4.5		2.5	%	
Differential output return loss			equation 83 EEE802.3br			
Common to differential mode conversion return loss		Per equation 83E-3 IEEE802.3bm				
Differential termination mismatch				10	%	
Transition time (min, 20% to 80%)		9.5			ps	
DC common mode voltage (min)		-350		2850	mV	4

Notes:

- 1. Maximum total power value is specified across the full temperature and voltage range.
- 2. With the exception to 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
- 3. Meets specified BER
- 4. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

IV. General Specifications

Parameter	Value	Unit	Notes
Module Form Factor	QSFP-DD		As defined by QSFP-DD
Number of Lanes	8 Tx and 8 Rx		
Maximum Aggregate Data Rate	425	Gb/s	
Maximum Data Rate per Lane	$26.5625 \pm 100 \text{ ppm}$	GBd	
Standard Cable Lengths	1, 2, 3, 5, 7, 10, 15, 20, 30, 50,	meters	Other lengths may be available upon
Protocols supported	70 200/400G Ethernet		request
Electrical Interface and Pin-out	76-pin edge connector		Pin-out as defined by QSFP-DD
Standard Optical Cable Type	Multimode round fiber cable,		Two options available: OFNR and Low
Standard Optical Cable Type	OM3/OM4		Smoke Zero Halogen (LSZH), or OFNP
Maximum Power Consumption per	ower Consumption per 8.5 (retimed Tx)		Maximum total power value is specified
End	(10000000000000000000000000000000000000	Watts	across the full temperature and voltage
			range
Management Interface	Serial, I2C-based, 1 MHz maximum frequency		As defined in CMIS 4.0

Data Rate Specifications	Symbol	Min	Тур	Max	Units	Ref.
Bit Rate per Lane	BR	$26.5625 \pm 100 \text{ ppm}$		GBd	1	
Pre-FEC Bit Error Ratio	BER			2.4E ⁻⁴		2

Notes:

- 1. Supports Ethernet
- 2. Tested with a PRBS 2³¹-1 test pattern.

V. Environmental Specifications

Coherent FCBx850QE2Cyy-1Y QSFP-DD Active Optical Cables have an operating case temperature range of 0°C to +70°C.

Parameter	Symbol	Min	Тур	Max	Units	Ref.
Case Operating Temperature	T_{op}	0		+70	°C	
Storage Temperature	T_{sto}	-40		+85	°C	1

1. Assumes no mechanical load force on the unit. Ensuring no mechanical load force requires a cable bend radius of >74 mm on the rest of the cable.

VI. Regulatory Compliance

The Coherent FCBx850QE2Cyy-1Y QSFP-DD Active Optical Cables are RoHS compliant. Copies of certificates are available from Coherent upon request.

Coherent FCBx850QE2Cyy-1Y QSFP-DD Active Optical Cables are Class 1 Laser Products. They are certified per the following standards:

Feature	Agency	Standard
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040.10 and Laser Notice 56
Laser Eye Safety	UL/CSA/TÜV	IEC/EN 60825-1:2014 IEC/EN 60825-2: 2004+A1+A2
Electrical Safety	UL/CSA/TÜV	IEC/UL/EN 62368-1:2014

CAUTION: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

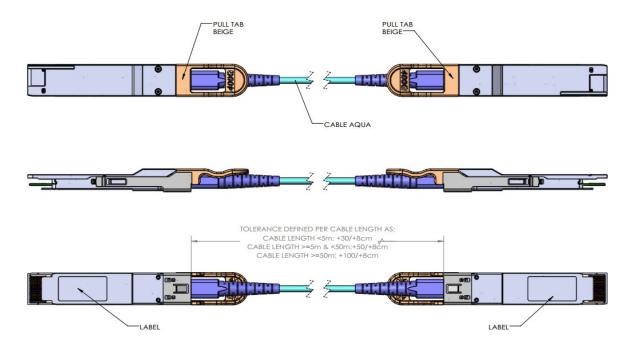
Either round-section construction LSZH, riser-rated or round-section construction, plennum-rated cable is alternative for Coherent FCBx850QE2Cyy-1Y QSFP-DD Active Optical Cables.

VII. Memory Map

Compatible with QSFP-DD CMIS rev 4.0.

VIII. Mechanical Specifications

Coherent FCBx850QE2Cyy-1Y QSFP-DD Active Optical Cables are compatible with the QSFP-DD Type 2 Specification for pluggable form factor modules.



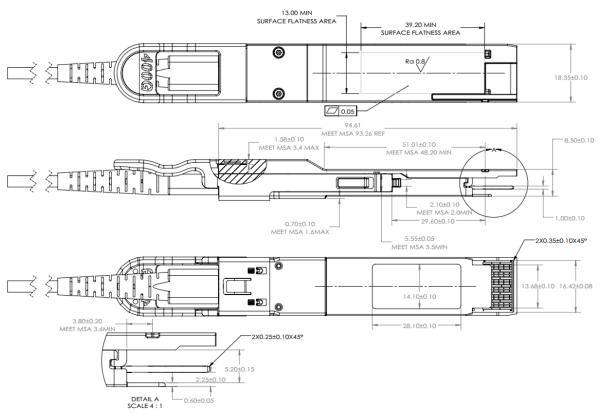


Figure 2. Mechanical Dimensions



Figure 3. Product Label

IX. References

- 1. QSFP-DD Hardware Specification for QSFP DOUBLE DENSITY 8X PLUGGABLE TRANSCEIVER Rev 5.0
- 2. SFF-8665: "QSFP+ 28Gb/s 4X Pluggable Transceiver Solution (QSFP28)", Rev 1.9, June 29, 2015 and associated SFF documents referenced therein:
 - i. SFF-8661
 - ii. SFF-8679
 - iii. SFF-8662
 - iv. SFF-8663
 - v. SFF-8672
- 3. Directive 2011/65/EU of the European Council Parliament and of the Council, "on the restriction of the use of certain hazardous substances in electrical and electronic equipment" as well as Commission Delegated Directive (EU) 2015/863 amending Annex II to Directive 2011/65/EU. Certain products may use one or more exemptions as allowed by the Directive.
- 4. Application Note AN-2038: "Coherent Implementation of RoHS Compliant Transceivers".
- 5. Common Management Interface Specification (CMIS) Rev 4.0.
- 6. IEEE P802.3bs, 400GAUI-8 Interface.

X. For More Information

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